Amendment To The Claims

1. (Canceled)

2. (Previously presented) The processor of Claim 49, including a first address indicator updating means and a second address indicator updating means,

the second address indicator updating means incrementing a value of the second address indicator in accordance with an amount of instructions that were executed in a preceding cycle and sending any carry generated in an incrementing to the first address indicator updating means, and

the first address indicator updating means adding the carry received from the second address indicator updating means to the value of the first address indicator.

3. (Previously presented) The processor of Claim 2, further including:

program counter relative value extracting means for extracting, when an instruction being executed includes a program counter relative value that is based on an address of a first instruction executed in a present cycle, the program counter relative value; and

calculating means for adding the program counter relative value to the value of the first address indicator and the value of the second address indicator, and setting an addition result as the value of the first address indicator and the value of the second address indicator.

4. (Previously presented) The processor of Claim 3, wherein the calculating means includes a first calculating unit and a second calculating unit,

the second calculating unit adding the value of the second address indicator and lower

bits of the program counter relative value, setting a result of an addition as the value of the second address indicator, and sending any carry generated in the addition to the first calculating unit,

the first calculating unit adding the value of the first address indicator, upper bits of the program counter relative value, and any carry received from the second calculating unit, and setting a result of an addition as the value of the first address indicator.

5. (Previously presented) The processor of Claim 3, wherein the calculating means includes a first calculating unit and a second calculating unit,

the second calculating unit adding the value of the second address indicator and lower bits of the program counter relative value without generating a carry, and setting a result of an addition as the value of the second address indicator,

the first calculating unit adding the value of the first address indicator and upper bits of the program counter relative value, and setting a result of an addition as the value of the first program counter.

6. (Previously presented) The program counter of Claim 3, wherein the calculating means adds the value of the first address indicator and upper bits of the program counter relative value, sets a result of an addition as the value of the first address indicator, and sets lower bits of the program counter relative value as the value of the second address indicator.

7. (Previously presented) The processor of Claim 3, wherein the calculating means adds the program counter relative value and a value whose upper bits are the value of the first

address indicator and lower bits are the value of the second address indicator, and sets upper bits of a result of an addition as the value of the first address indicator and lower bits of the result as the second address indicator.

8. (Previously presented) The processor of Claim 2, further including:

program counter relative value extracting means for extracting, when an executed instruction includes a program counter relative value that is based on an address of the executed instruction, the program counter relative value;

program counter amending means for amending the value of the first address indicator and the value of the second address indicator to indicate an address of the executed instruction; and

calculating means for adding the program counter relative value, the value of the first address indicator, and the value of the second address indicator, and setting a result of an addition as the value of the first address indicator and the value of the second address indicator.

9. (Previously presented) The processor of Claim 2, further including:

program counter relative value calculating instruction decoding means for decoding a program counter relative value calculating instruction that performs an addition using a program counter relative value and one of

(a) a value of the program counter stored in a register, and

(b) the value of the first address indicator and the value of the second address indicator;

calculating means for performing the addition indicated by the program counter relative value calculating instruction to generate an addition result; and

program counter value updating means for storing the addition result in one of

(a) the register, and

(b) the first address indicator and the second address indicator.

10. (Previously presented) The processor of Claim 49, wherein the first address indicator indicates bits of a memory address more significant than a $1 + log_2 n^{th}$ bit from a least significant, the memory address specifying the storage position of the processing packet in memory, and n being a length of a processing packet in bytes.

11. (Previously presented) The processor of Claim 10, further including

an instruction buffer for temporarily storing instructions; and

instruction reading means for transferring instructions being made of an integer number of bytes from the memory to the instruction buffer, in accordance with available space in the instruction buffer but regardless of a size of a processing packet.

12-48. (Canceled)

49. (Currently Amended) A processor for reading instructions from a memory comprising:

a memory configured to store, in a position corresponding to a byte boundary, at least one processing packet ~~being made of~~ having a natural number of bytes, the processing packet including a predetermined number of processing target instructions, each processing target

instruction being an operation to be executed by the processor, the number of processing target instructions being any natural number except for a power of 2;

a first address indicator configured to indicate a storage position of the processing packet in the memory; and

a second address indicator configured to indicate a position of a processing target instruction ~~in~~ within the processing packet by using the same number of positions as the predetermined number of processing target instructions, and cycling through the positions within the processing packet by an increment value,

wherein after the second address indicator finished cycling through the positions, the first address indicator indicates ~~the~~ a next storage position of ~~the~~ another processing packet in the memory.

50-51. (Cancelled)